A drive impedance **230**, **240** is shown coupled between the external drive circuit **220** and the gate of the composite FET **200**. The drive impedance **230**, **240** may include one or more discrete impedance elements, the output impedance of the external drive circuit, impedance of one or more physical connection and/or the like. In one implementation, the drive impedance **230**, **240** coupled between the external drive circuit and the gate of the composite FET **200** may include a resistive **230** and a capacitive **240** element. Furthermore, a load impedance **250** is shown coupled between the high voltage source **210** and the drain of the composite FET **200**. The load impedance **250** may be included to limit the current flowing between the source and drain of the switching device so that the device is not damaged due to an over current condition. The load impedance **250** may represent the effective impedance of a circuit that the composite FET **200** is coupled to, and/or include a discrete impedance element, the output impedance of the supply **210**, impedance of one or more physical connections and/or the like.

The composite FET **200** includes a depletion mode JFET **260** (Q**1**), an enhancement mode N-channel MOSFET **270** (Q**2**) and a zener diode **280** (CR**1**). The drain of the JFET **260** is coupled to the drain of the composite FET **200**. The source of the JFET **260** is coupled to the drain of the MOSFET **270**. The source of the MOSFET **270** is coupled to the source of the composite FET **200**. The anode of the zener diode **280** is coupled to the gate of the JFET **260** and the cathode of the zener diode **280** is coupled to the gate of the MOSFET **270**. The gate of the MOSFET **270** is also coupled to the gate of the composite FET **200**.

The composite FET **200** has an "on" and "off" state. In the off state (e.g., initial conditions) the gate-to-source voltage ($V_{GS(Q2)}$) of the MOSFET **270** is substantially 0V. The drain-to-source voltage ($V_{DS(Q2)}$) of the MOSFET **270** may be assumed to be a voltage sufficient to cause the channel of the JFET **260** to pinch off. The JFET may be pinched off when $V_{DS(Q2)}=V_{GS(Q1)PINCHOFF}$+0.7V, wherein 0.7V is the forward drop of CR**1**. When the external driver circuit **220** turns on, the drive potential (LDRV) raises, charging the input capacitance ($C_{ISS(Q2)}$) of the MOSFET **270**. Once the gate-to-source potential (VGS(Q**2**)) of the MOSFET **270** has risen above its threshold (e.g., $V_{T(Q2)}$=1.0V), the channel of the MOSFET **270** will conduct. This will cause the potential at the drain of the MOSFET **270** to pull towards the potential at the source of the MOSFET **200** (e.g., PGND=0V), and will begin to charge the input capacitance ($C_{ISS(Q1)}$) of the JFET **260** through the zener diode **280**. The drive potential ($V_{LDVR}$) will then be providing current to charge the input capacitance ($C_{ISS(Q1)}$) of the JFET **260** as soon as there is sufficient potential on the gate of the MOSFET **270** to overcome the breakdown voltage ($V_{Z(CR1)}$) of the zener diode **280**.

As the input capacitance ($C_{ISS(Q1)}$) of the JFET **260** charges up, the channel of the JFET **260** begins to turn on. At this point the MOSFET **270** is already fully enhanced, and the input capacitance ($C_{ISS(Q1)}$) of the JFET **260** is being charged by the drive circuit **220** through the capacitive element **270** of the input impedance **230**, **240**. When the gate-to-source voltage ($V_{GS(Q1)}$) of the JFET **260** reaches the threshold voltage (e.g., $V_{T(Q2)}$=0.7V) of the JFET **260**, the gate-to-source junction will clamp, which will in turn clamp the voltage at the gate of the composite FET **200** to 0.7V+$V_{Z(CR1)}$. The resistive element **270** of the input impedance **260**, **270** will then provide gate current to inject: minority carriers into the JFET **260**, thereby improving its conductivity, especially at high drain currents.

In the steady state on state of the composite FET **200**, the gate-to-source potential of the MOSFET **270** is at 0.7V+$V_{Z(CR1)}$ (e.g., about 5V), and the JFET **260** and MOSFET **270** are both conducting. In addition, the input capacitance **270** is charged to approximately 7V (e.g., $V_{PDRV}$–(0.7+$V_{Z(CR1)}$)).

When the external driver circuit **220** pulls low (e.g., turn-off), the zener diode **280** conducts, discharging the gate of the JFET **260** (e.g., $C_{ISS(Q1)}$) and pulling its voltage towards PGND. The external driver simultaneously discharges the gate of MOSFET **270**, causing it to turn off. The input capacitance ($C_{ISS(Q1)}$) of the JFET **260** discharge path is through the channel of the MOSFET **270** initially, then through the body diode of the MOSFET **270**, and also flows through zener diode **280**, the drive impedance **230**, **240**, and through driver circuit **220**. When the channel of the JFET **260** turns off, the drain of the JFET **260** will rise, forcing additional current back through the drain-to-gate capacitance ($C_{GD(Q1)}$) of the JFET **260** whose discharge current flows through Zener diode **280**, capacitance **270** and finally through driver circuit **220** to PGND. When the channel of the MOSFET **270** turns off, the source of the JFET **260** will rise, causing current that is provided by the gate-to-source capacitance ($C_{GS(Q1)}$) of the JFET **260** also to be discharged through the zener diode **280** capacitance **270** and finally through driver circuit **220** to PGND. When the MOSFET **270** drain potential reaches a voltage sufficient to pinch off JFET **260**'s gate the circuit is fully off with JFET **260** blocking the high voltage and MOSFET **270** blocking sufficient voltage to keep JFET **260** off.

The zener diode **280** causes the n-channel MOSFET **270** to become enhanced before gate current is provided to the depletion mode JFET **260**. In addition, the zener diode **280** allows the gate current in the JFET **260** to flow in both directions to rapidly switch the JFET **260**. The zener diode **280** also advantageously clamps the potential at the gate of the MOSFET **270**, protecting its oxide from potential rupture thus allowing a thin gate oxide to be used. This improves the on resistance ($R_{DS(ON)}$) of the MOSFET **270**. The breakdown voltage of the zener diode **280** can also be controlled, allowing the gate drive characteristics of the composite FET **200** to be optimized to the application.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.

What is claimed is:

**1**. A composite field effect transistor comprising:

a zener diode;

a junction field effect transistor having a gate coupled to an anode of the zener diode;

a metal-oxide-semiconductor field effect transistor having a gate directly connected to a cathode of the zener diode and having a drain directly connected to a source of the junction field effect transistor.

**2**. The composite field effect transistor of claim **1**, wherein the junction field effect transistor comprises a depletion mode junction field effect transistor.